Interfacing to the Booster BLM Upgrade Integrator/Digitizer VME Module INTEG03

Revised February 17, 2011

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I. Introduction

The Integrator/Digitizer Card is a 4 channel 6U VME module used to integrate and digitize charge generated by a Beam Loss Monitor. This module is to be used in the Tevatron and the Main Injector as well as in the Booster. The application in the Booster is different than in the other machines since abort logic functions supported by the module are not used in the Booster. Also, there are four other modules that are part of the BLM Upgrade project that are used in the Tevatron and the Main Injector, and not in the Booster. This note will describe the functions of the Integrator/Digitizer Card as they are expected to be used by the Booster.

Quick Start for Module Testing

For the MVME 2301 the VME address, for a particular register, is the offset to the VME memory space 0xfa000000 plus the board number shifted left 20 times plus the register offset.

1. Ensure that DIP switch 7 is up (logic high) and switches 5 and 6 are down (logic low). Switches 1 through 4 should be set to the desired 4 bit Board Number (0 through 15).
2. Write the Alternate Integrator Control register at address offset 0x01034 to turn off the front panel input and turn on the Test input for the channel or channels you wish to use. Write 0xff00 to address offset 0x1034 for all four channels. See Table III.6.
3. Set the Test input by writing the Test DAC Setting register at address offset 0x01048.
4. Start a 40 ms data acquisition cycle by writing anything to address offset 0x01010.
5. Read the data collected in the FIFO's at the following address offsets

Channel 1 Data	0x01020
Channel 2 Data	0x01022
Channel 3 Data	0x01024
Channel 4 Data	0x01026

II. Charge Integration and Digitization

The Integrator/Digitizer Card (DC) integrates and digitizes the current from four loss monitor chambers every 20 μs. To avoid dead time between measurements, signals for each input are switched between the two channels of a TI/Burr-Brown ACF2101

integrator chip. Results are digitized from the two channels on alternate cycles and fed to on-board programmable logic devices.

The digitizer has a 16 bit resolution. Scaling is such that one digitizer count represents 15.26 fC of charge in the integrator. The sensitivity of the BLM ion chamber is approximately 70 nC of charge per Rad. The analog to digital converters used are Analog Devices AD7654's.

II.1 Scaling Digitizer Values to Rads and Rads/Second

The sealed ion chamber used in the Booster has a scale factor of 70 nano-Coulombs per Rad of radiation that passes though its cross section. The charge produced by the ion chamber is accumulated in the BLM integrating amplifiers. The integration capacitor in the normal operating mode is 100 pF, and the full scale output of the integrator is 10 Volts. Therefore the full scale output in Coulombs is

The integrator voltage is digitized with a 16 Bit ADC giving

Applying the relationship between Rads and the Coulombs of charge produced by the Loss Monitor Ion chamber we get

This is the conversion before we *average* four integration intervals together and store the average in the FIFO from which the processor gets its values. Therefore the conversion that is to be applied to the values read from the FIFO's by the processor is

The measurement made is an integration or summing of charge from the Loss Monitor ion chamber. If we wish to compute Rad/Second, the rate at which radiation is impacting the ion chamber, we must settle for the average rate over some time interval. The smallest time interval is the 20.0 μs interval that the digitized integrator values represent. Since the values written to the FIFO's is the average value over 4 each 20.0 μs intervals one can compute the Rads/Sec rate these values describe

III. VME Interface

The VME interface is implemented using the upper J1/P1 backplane connection. The lower J2/P2 backplane connection is used as an application specific Control Bus and Abort Bus in applications other than the Booster.

Take note that the "A" and "C" rows of the J2/P2 connection have been assigned and other boards in the crate that are not part of the BLM Upgrade project should not be inserted into the crate with the Integrator/Digitizer Card if they use these pins. The exceptions to this rule are when the J2/P2 backplane of the crate does not bus the "A" and "C" rows (a common configuration), or if the non-BLM Upgrade board is used in slots 1 through 4 in a crate using the BLM Upgrade custom J2/P2 backplane. The "A" and "C" rows are not bussed to slots 1 through 4 of the custom backplane.

The VME data transfer modes supported are A24D16 modes.

Standard Supervisory Block Transfer,	AM[5..0] = 3F
Standard Supervisory program access,	AM[5..0] = 3E
Standard Supervisory data access,	AM[5..0] = 3D
Standard Non-privileged Block Transfer,	AM[5..0] = 3B
Standard Non-privileged program access,	AM[5..0] = 3A
Standard Non-privileged data access,	AM[5..0] = 39

Program access is treated exactly the same as data access. Supervisory modes are treated exactly the same as non-privileged modes. Block transfers can be supported with some adjustment to the FPGA firmware. Block transfers are not support as of the writing of this note.

The 24 VME address lines are used as follows. The most significant 4 bits (A23 to A20) are compared to DIP switches on the module to determine if the particular board is being addressed. The 19 bits, A19 to A1, are used to address memory and registers for the selected module.

Table III.1 Integrator / Digitizer VME Memory Map

Register / Command / Memory	**Address [19..0]**	**R/W**	**Description**
Board ID Memory (ROM)	0x00000 to 0x001FE	R	Board ID number and text string. (1 character per 16 Bit word.)
Board Serial Number	0x00200 to 0x00206	R	Board Serial Number from the DS2401 ROM. device, 64 Bits.
Firmware Version Number	0x00208 to 0x0021E	R	Not Used
unused	0x00220 to 0x00FFE	--	
Internal Registers and Control	0x01000 to 0x0FFFE	--	**See Table III.2**
Upper SRAM Memory	0x10000 to 0x4FFFE	R/W	
unused	0x50000 to 0x7FFFE	--	
Lower SRAM Memory	0x80000 to 0xBFFFE	R/W	

Table III.2 Internal Registers and Control.

Register / Command / Memory	**Address [19..0]**	**R/W**	**Description**
Command Register	0x01000	--	See Table III.3
Reserved	0x01002 Thru 0x0100E	--	
Start DAQ Command	0x01010	W	By writing this address the module is commanded to **start** a 40 ms data acquisition interval.
Reserved	0x01012	--	
Clear FIFO Command	0x01014	W	By writing this address the module is commanded to clear the data FIFO's.
Record Length Register	0x01016	R/W	Not Currently Used
Channel 1 Data FIFO	0x01020	R	Data FIFO output port. This FIFO channel is also mapped to the address range 0x01200 to 0x013FF.
Channel 2 Data FIFO	0x01022	R	Data FIFO output port. . This FIFO channel is also mapped to the address range 0x01400 to 0x015FF.
Channel 3 Data FIFO	0x01024	R	Data FIFO output port. . This FIFO channel is also mapped to the address range 0x01600 to 0x017FF.
Channel 4 Data FIFO	0x01026	R	Data FIFO output port. . This FIFO channel is also mapped to the address range 0x01800 to 0x019FF.
Number of Records in Channel 1 FIFO	0x01028	R	
Number of Records in Channel 2 FIFO	0x0102A	R	
Number of Records in Channel 3 FIFO	0x0102C	R	
Number of Records in Channel 4 FIFO	0x0102E	R	
FIFO Status Register	0x01030	R	See Table III.4
Alternate Integrator Control Register 1	0x01032	R/W	See Table III.5
Alternate Integrator Control Register 2	0x01034	R/W	See Table III.6
Data Average Length Register	0x01036	R/W	Channels are averaged using this number of samples.
Channel 1 Average Register	0x01038	R	
Channel 2 Average Register	0x0103A	R	
Channel 3 Average Register	0x0103C	R	
Channel 4 Average Register	0x0103E	R	
Reserved	0x01040 Thru 0x01046	--	
Test DAC Setting Register	0x01048	R/W	Setting for the Test DAC. Full scale output is 0x7FFF
Channel 1 FIFO Baseline	0x0104A	R	
Channel 2 FIFO Baseline	0x0104C	R	
Channel 3 FIFO Baseline	0x0104E	R	
Channel 4 FIFO Baseline	0x01050	R	

Table III.3 Command Register:

Bit	Description
0	Error signal J2
1	USE_ALT_REG_1: Use the Alternate Integrator Control Signal Register 1. This is a VME controlled register used to manipulate the individual integrator Hold, Select, and Reset switches integral to the Burr Brown ACF2101 dual integrators.
2	Disable Baseline Subtraction: When set High the baseline subtraction is not applied to the FIFO data.
3	Un-assigned
5 … 4	Test Vector Select Bits
15 … 6	Un-assigned

Table III.4 FIFO Status Register:

Bit	Description
0	FIFO Channel 1 Full.
1	FIFO Channel 1 Empty.
2	FIFO Channel 2 Full.
3	FIFO Channel 2 Empty.
4	FIFO Channel 3 Full.
5	FIFO Channel 3 Empty.
6	FIFO Channel 4 Full.
7	FIFO Channel 4 Empty.
8	undefined
9	undefined
10	undefined
11	undefined
12	undefined
13	undefined
14	undefined
15	undefined

Table III.5 Alternate Integrator Control Register 1:

Bit	Description
NOTE:	**This register is enabled only if Bit 1 of the Command Register is High.** Logic has been arranged so that these signals are active high logic even though some of the associated signals on the PCB are active low logic.
0	HOLD_B_12: Hold off the output of Channel 1 and 2 side B.
1	SEL_B_12: Select Channel 1 and 2 side B for digitization.
2	RESET_B_12: Reset the B side integrators on Channels 1 and 2.
3	HOLD_B_34: Hold off the output of Channel 3 and 4 side B.
4	SEL_B_34: Select Channel 3 and 4 side B for digitization.
5	RESET_B_34: Reset the B side integrators on Channels 3 and 4.
6	HOLD_A_12: Hold off the output of Channel 1 and 2 side A.
7	SEL_A_12: Select Channel 1 and 2 side A for digitization.
8	RESET_A_12: Reset the A side integrators on Channels 1 and 2.
9	HOLD_A_34: Hold off the output of Channel 3 and 4 side A.
10	SEL_A_34: Select Channel 3 and 4 side A for digitization.
11	RESET_A_34: Reset the A side integrators on Channels 3 and 4.
12 … 15	Not Defined

Table III.6 Alternate Integrator Control Register 2:

Bit	**Description**
NOTE:	**This register is enabled only when DIP switch SW7 is High.** Logic has been arranged so that these signals are active high logic even though some of the associated signals on the PCB are active low logic.
0	HI_RNG_1_12: Switch the integrating capacitor to 500 pF in Channel 1.
1	HI_TAU_1_12: Switch additional 16k Ohm resistor in series with input for Channel 1.
2	HI_RNG_2_12: Switch the integrating capacitor to 500 pF in Channel 2.
3	HI_TAU_2_12: Switch additional 16k Ohm resistor in series with input for Channel 2.
4	HI_RNG_1_34: Switch the integrating capacitor to 500 pF in Channel 3.
5	HI_TAU_1_34: Switch additional 16k Ohm resistor in series with input for Channel 3.
6	HI_RNG_2_34: Switch the integrating capacitor to 500 pF in Channel 4.
7	HI_TAU_2_34: Switch additional 16k Ohm resistor in series with input for Channel 4.
8	TEST_1_12: Switch the Test Input on for Channel 1.
9	TEST_2_12: Switch the Test Input on for Channel 2.
10	TEST_1_34: Switch the Test Input on for Channel 3.
11	TEST_2_34: Switch the Test Input on for Channel 4.
12	INPUT_1_12: Switch front panel signal into integrator for Channel 1.
13	INPUT_2_12: Switch front panel signal into integrator for Channel 2.
14	INPUT_1_34: Switch front panel signal into integrator for Channel 3.
15	INPUT_2_34: Switch front panel signal into integrator for Channel 4.

IV. Diagnostics

The INTEG03 board has a couple operating modes. DIP Switches, which are not used as board address bits, serve to select between modes for the board. These switches are shown in Figure IV.1.

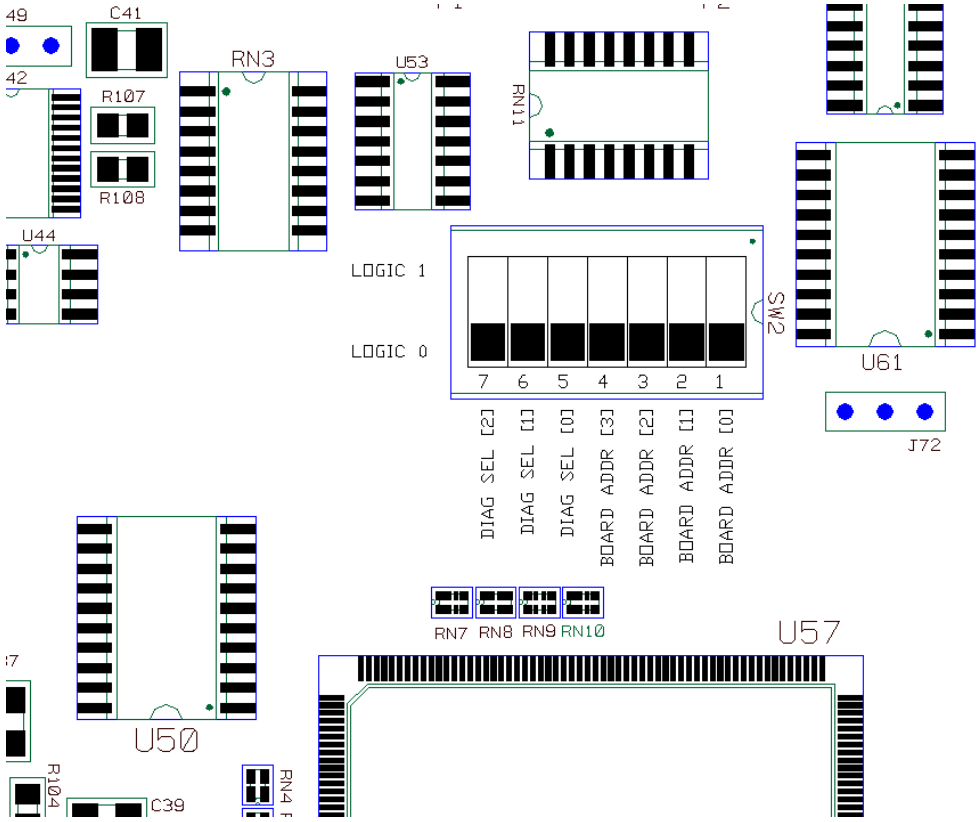

Figure IV.1 The Select switch for board address and diagnostic mode selection.

The normal mode for the module has SW7, SW6 and SW5 all in the Logic 0 position. In this mode integrator data is gated into the FIFO memories for 40 ms after the rising edge on Trigger Input T1. After 40 ms has elapsed, the FIFO's are no longer written, but the integrators continue to run. When the next T1 trigger occurs, the FIFO's are cleared before new data is written to them.

If SW7 is set to the Logic 1 position the T1 trigger will no longer have an effect. The starting of data taking is now controlled by the crate processor writing to address offset 0x01010. A write to this address will trigger a new 40 ms DAQ cycle as described above and will start the integrators if they are not already running.

If SW6 is set to the Logic 1 position a baseline subtraction process is enabled. When the 40 ms DAQ interval is not active digitized integrator values are averaged (typically an average of 16 points) and stored in a baseline register for each channel. During the 40 ms DAQ interval the values in the baseline registers is subtracted from the measured integrator values before writing them to the FIFOs.

If SW5 is set to the Logic 1 position test data from ROM memory is written to the FIFO memory instead of the integrator measurements. Baseline subtraction is also disabled with SW5 in this position.

The figure below shows most of the integrator test points and balancing pots.

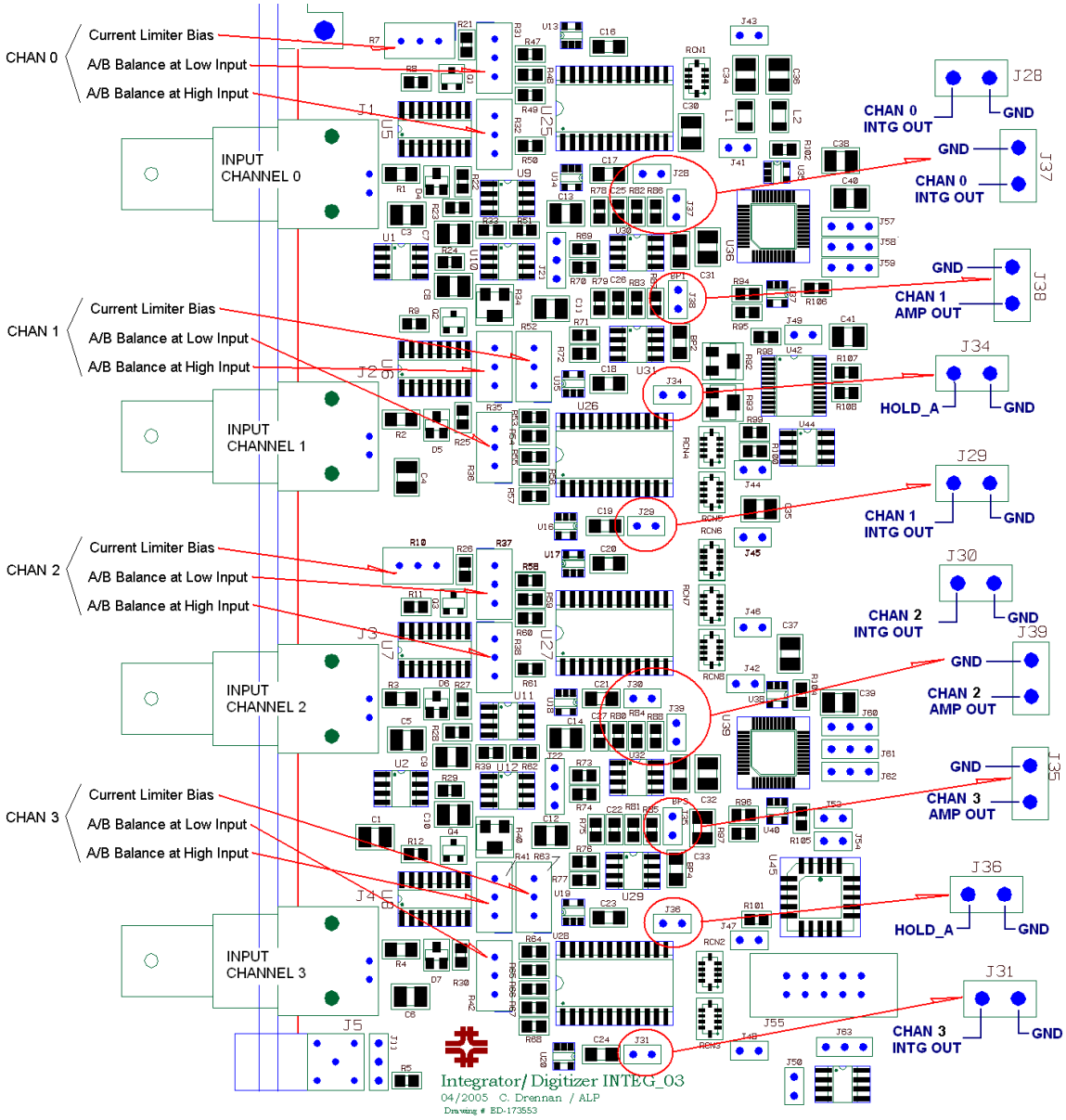

Figure IV.2 Test points and Adjustments.

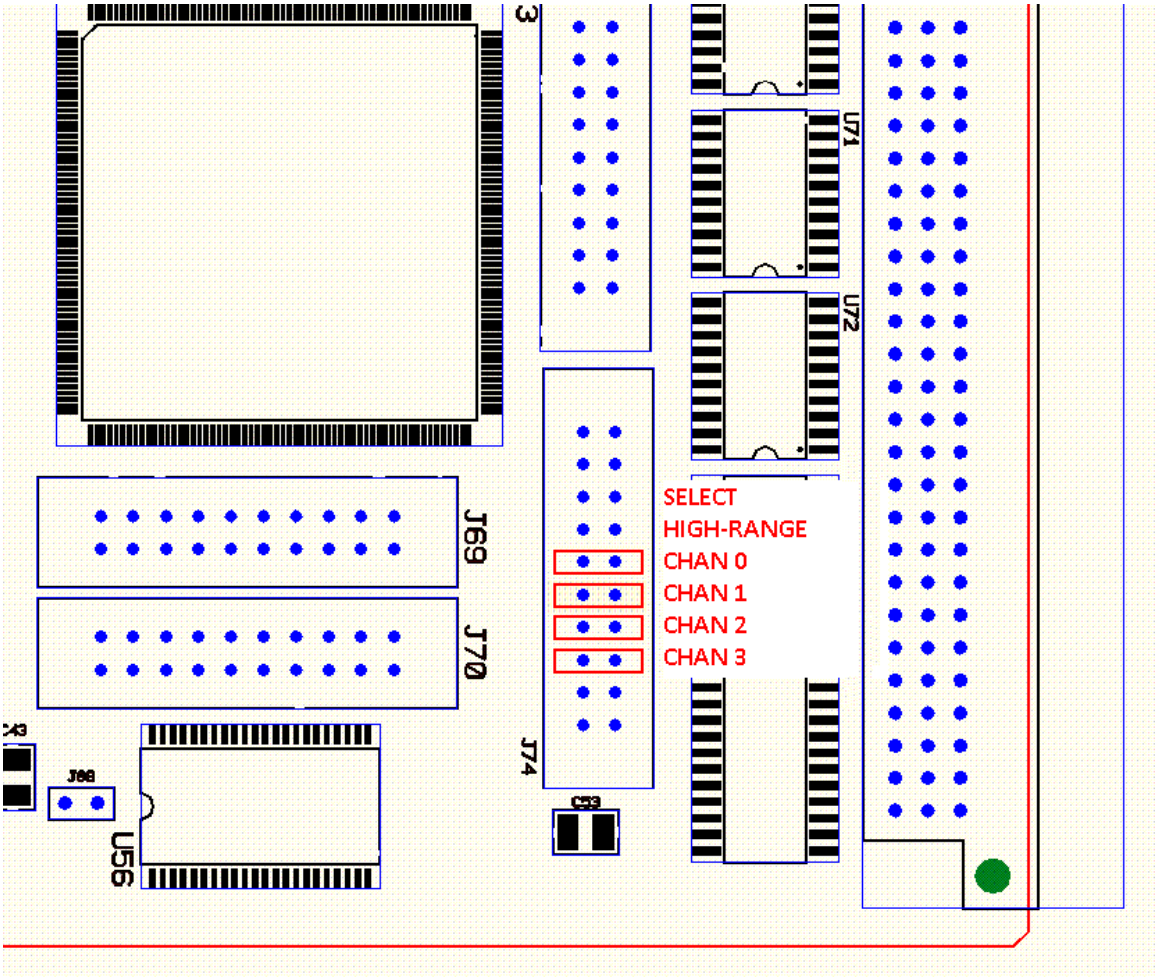

Figure IV.3 Jumper selection of High-Range Mode.